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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,284	CHILTON, KENDELL A.	
	Examin r	Art Unit	
	David J. Huisman	2183	

-- Th MAILING DATE of this communication app ars on th cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 12/3/2004.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

In Fig.6, number 126-3.

Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Maintained Rejections

4. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Maintained Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-5, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Sharangpani et al., U.S. Patent No. 6,237,077 (herein referred to as Sharangpani).

6. Referring to claim 1, Sharangpani has taught in a memory circuit board that stores a cache for a data storage system (see column 7, lines 12-13 and note that a cache has been implemented and clearly, this cache would be on a circuit board), a method comprising the steps of:

a) receiving a communication that includes a script command and a payload, the payload including a series of individual instructions. See Fig.2 and column 4, lines 54-57, and note the existence of a script command (field 220) and a payload (fields 210a-c), where the payload includes 3 instructions.

b) in response to the script command, parsing the payload to identify the series of individual instructions. See the abstract and Table 2 in column 6. Note that based on the template, the instructions and their types are determined and then they are routed to execution units.

c) performing a series of operations in accordance with the identified series of individual instructions. Clearly, each of the instructions in the payload will be executed by the appropriate execution units (those shown in Table 1 in column 5).

7. Referring to claim 4, Sharangpani has taught a method as described in claim 1. Sharangpani has further taught that the steps of parsing and performing occur as an atomic operation. See Fig.4A and note that the instruction packets are executed in order. That is, a first packet is parsed and executed, a second packet is parsed and executed, etc. The first packet's execution is not interrupted by the second packet's execution. Therefore, the parsing and performing steps are atomic.

8. Referring to claim 5, Sharangpani has taught a method as described in claim 1. Sharangpani has further taught the steps of:

a) generating a series of results in response to performing the series of operations. Clearly, instructions that are performed will generate results.

b) providing the series of results to a processor circuit board. See column 4, lines 6-11. When a result is generated, it is generally stored so it may be used in some way in the future. Usually, the data is stored in a register, which is storage on the processor board.

9. Referring to claim 7, Sharangpani has taught a method as described in claim 1. Sharangpani has further taught loading a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations. Note from Fig.1A that load instructions exist within Sharangpani's system. As is known, load instructions load registers with data (constants) which are used as operands (parameters) in later instructions such as Add instructions.

Maintained Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani, as applied above, in view of Hennessy and Patterson, Computer Architecture - A Quantitative Approach, 2nd Edition, 1996 (herein referred to as Hennessy).

12. Referring to claim 2, Sharangpani has taught a method as described in claim 1. Sharangpani has taught an instruction cache (as described in the rejection of claim 1) but has not explicitly taught a data cache, wherein the data cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the step of performing the series of operations includes the steps of:

a) selecting the data element based on the address of the individual instruction.

b) retrieving the data element from the memory locations of the cache.

c) performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

However, Official Notice is taken that data caches and the method of accessing data caches are well known concepts in the art. The examiner asserts that the claimed steps set forth in claim 2 are the known and expected steps used to access a data cache. More specifically, when an instruction is to access memory for an operand, such as the

Add R1, (1001) instruction shown on page 75 of Hennessy, the processor will first look to the cache for the operand stored in memory location 1001. If it is in the cache, then the access to main memory may be avoided, thereby resulting in faster operand retrieval because caches are faster than main memory (due in part to their close proximity to the CPU). The operand is then used in the operation specified by the instruction (in this case, an addition operation). Hennessy has taught on page 75 that such an instruction would be useful in accessing static data and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharangpani to include this instruction. Furthermore, to increase data retrieval speed, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharangpani to include a data cache and a method for accessing the data cache as described above.

13. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani, as applied above, in view of Narayan et al., U.S. Patent No. 5,748,978 (herein referred to as Narayan).

14. Referring to claim 3, Sharangpani has taught a method as described in claim 1. Sharangpani has not taught that the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the step of performing the series of operations includes the steps of:

a) referencing the section of the code of the instruction library based on the instruction reference.

b) executing the section of code.

However, Narayan has taught the implementation of an MROM unit, which as discussed in column 8, lines 10-19, is used to break down complex instructions into smaller, less complicated routines, which are then executed to perform the operation specified by the complex instruction. Clearly, if an instruction is broken down into a set of smaller instructions, then the instruction will determine which set of instructions are executed. As discussed, an MROM is hardware used to efficiently decode complex instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sharangpani to include an MROM unit.

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani, as applied above, and further in view of Abdallah et al., U.S. Patent No. 6,233,671 (herein referred to as Abdallah).

16. Referring to claim 6, Sharangpani has taught a method as described in claim 1. Sharangpani has not taught that the step of providing the series of results to the processor circuit board includes the steps of:

a) packaging the series of results in a set of data blocks; and

b) transferring the set of data blocks to the processor circuit board.

However, Abdallah has taught such a concept. See Fig.3 for instance and note that multiple operations are performed in parallel, and the results are packaged together and stored in a register on the processor board. And, from column 4, lines 5-6, note that it only takes a single write to write the packed results. This is clearly advantageous in that multiple writes would not be required, thereby making the processor more efficient. As a result, it would have been obvious to one of ordinary skill in the art at the time of

the invention to modify Sharangpani to package a series of results and transfer them to the processor board.

17. Claims 8, 11-12, 14-15, 18-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein referred to as AAPA), in view of Lemmon, U.S. Patent No. 5,278,974 (herein referred to as Lemmon), and further in view of Sharangpani, as applied above.

18. Referring to claim 8, AAPA has taught a data storage system comprising:

a) a set of storage devices. See page 1, lines 6-10 of applicant's background.

b) a memory circuit board that stores a cache to temporarily store copies of data elements stored in the set of storage devices. See page 1, lines 6-10 of applicant's background.

c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices (see page 1, line 11, to page 2, line 4, of applicant's background).

d) Applicant has further taught the sending of instructions, one at a time, to the memory circuit board, where the operation specified by the instruction is performed. See page 2, lines 5-17, of applicant's background. Applicant has not explicitly taught packing multiple instructions together and transmitting them to the memory circuit board at a single time. More specifically, applicant has not taught that the memory circuit board is configured to:

> (i) receive, from the processor circuit board, a communication that includes a script command and a payload, the payload including a series of individual instructions.

(ii) parse the payload to identify the series of individual instructions in response to the script command.

(iii) perform a series of operations in accordance with the identified series of individual instructions.

However, Lemmon has taught (and supported a well known concept), that some amount of overhead is required for every data transfer that is required. A person of ordinary skill in the art would have recognized that by packaging multiple items (in this case instructions) into a single "packet" and then transmitting the packet, the overall number of data transfers will be reduced. For instance, if six instructions need to be transferred, and if one transfer may be performed every time unit, then six time units would be required to perform six individual transfers. On the other hand, if a packet is able to hold three instructions, then only two transfers will need to be made, resulting in four less time units required to perform the transfer. Clearly, the amount of transfer time is reduced, and as a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA to package multiple instructions and transfer them together.

Sharangpani has taught that an instruction packet includes a script command and a payload, the payload including a series of individual instructions. See Fig.2 and column 4, lines 54-57, and note the existence of a script command (field 220) and a payload (fields 210a-c), where the payload includes 3 instructions. Furthermore, in response to the script command, Sharangpani has taught parsing the payload to identify the series of individual instructions. See the abstract and Table 2 in column 6. Note that based on the template, the instructions and their types are determined and then they are routed to

execution units. Finally, Sharangpani has taught performing a series of operations in accordance with the identified series of individual instructions. Clearly, each of the instructions in the payload will be executed by the appropriate execution units (those shown in Table 1 in column 5). A person of ordinary skill in the art would have recognized that if a packet of instructions is transmitted, then the packet must include instructions (payload), and the script (template in Sharangpani) is beneficial to have since it allows for rapid issuing of the associated instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA in view of Lemmon to include a packet which contains multiple instructions (payload) and a template (script command).

19. Referring to claim 11, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 8. AAPA in view of Lemmon and further in view of Sharangpani has further taught that the memory circuit board is configured to receive the communication, parse the payload, and perform the series of operations as an atomic operation. If something is "atomic" then it must be fully completed and it must not be interrupted. Clearly, the communication, parsing, and execution of instructions must be fully completed or else the overall program would not be executed correctly. In addition, Sharangpani shows no signs of interruption of communicating, parsing, and executing instructions. In fact, according to Fig.4A, instruction packets are executed in order. That is, a first packet is parsed and executed, a second packet is parsed and executed, etc. The first packet's execution is not interrupted by the second packet's execution.

20. Referring to claim 12, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 8. Furthermore, the method of claim 5 is performed by the system of claim 12. Therefore, claim 12 is rejected for the same reasons set forth in claim 5.

21. Referring to claim 14, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 8. Furthermore, the method of claim 7 is performed by the system of claim 14. Therefore, claim 14 is rejected for the same reasons set forth in claim 7.

22. Referring to claim 15, AAPA has taught a memory circuit board for a data storage system, comprising:

a) an input/output port to connect with a processor circuit board of the data storage system. Clearly, if a processor is connected to a memory, and data travels between the two, then an input/output port inherently exists because data is inputted from memory and outputted to memory.

b) a set of memory locations to hold a cache that temporarily stores copies of data elements stored in a set of storage devices of the data storage system. See page 1, lines 6-10 of applicant's background.

c) Applicant has further taught the sending of instructions, one at a time, to the memory circuit board, where the operation specified by the instruction is performed. See page 2, lines 5-17, of applicant's background. Applicant has not explicitly taught packing multiple instructions together and transmitting them to the memory circuit board at a single time. More specifically, applicant has not taught that the memory circuit board is configured to:

(i) receive, from the processor circuit board through the input/output port, a communication that includes a script command and a payload, the payload including a series of individual instructions.

(ii) parse the payload to identify the series of individual instructions in response to the script command.

(iii) perform a series of operations in accordance with the identified series of individual instructions.

However, Lemmon has taught (and supported a well known concept), that some amount of overhead is required for every data transfer that is required. A person of ordinary skill in the art would have recognized that by packaging multiple items (in this case instructions) into a single "packet" and then transmitting the packet, the overall number of data transfers will be reduced. For instance, if six instructions need to be transferred, and if one transfer may be performed every time unit, then six time units would be required to perform six individual transfers. On the other hand, if a packet is able to hold three instructions, then only two transfers will need to be made, resulting in four less time units required to perform the transfer. Clearly, the amount of transfer time is reduced, and as a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA to package multiple instructions and transfer them together.

Sharangpani has taught that an instruction packet includes a script command and a payload, the payload including a series of individual instructions. See Fig.2 and column 4, lines 54-57, and note the existence of a script command (field 220) and a payload (fields 210a-c), where the payload includes 3 instructions. Furthermore, in response to

the script command, Sharangpani has taught parsing the payload to identify the series of individual instructions. See the abstract and Table 2 in column 6. Note that based on the template, the instructions and their types are determined and then they are routed to execution units. Finally, Sharangpani has taught performing a series of operations in accordance with the identified series of individual instructions. Clearly, each of the instructions in the payload will be executed by the appropriate execution units (those shown in Table 1 in column 5). A person of ordinary skill in the art would have recognized that if a packet of instructions is transmitted, then the packet must include instructions (payload), and the script (template in Sharangpani) is beneficial to have since it allows for rapid issuing of the associated instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA in view of Lemmon to include a packet which contains multiple instructions (payload) and a template (script command).

23. Referring to claim 18, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 15. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 11.

24. Referring to claim 19, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 15. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 12.

25. Referring to claim 21, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 15. Furthermore, claim 21 is rejected for the same reasons set forth in the rejection of claim 14.

26. Referring to claim 22, AAPA has taught a processor circuit board for a data storage system, comprising:

a) an input/output port to connect with a memory circuit board of the data storage system. Clearly, if a processor is connected to a memory, and data travels between the two, then an input/output port inherently exists because data is inputted from memory and outputted to memory.

b) Applicant has further taught the sending of instructions, one at a time, to the memory circuit board, where the operation specified by the instruction is performed. See page 2, lines 5-17, of applicant's background. Applicant has not explicitly taught packing multiple instructions together and transmitting them to the memory circuit board at a single time. More specifically, applicant has not taught control circuitry coupled to the input/output port, wherein the control

circuitry is configured to provide, to the memory circuit board through the input/output port, a communication that includes a script command and a payload, wherein the payload includes a series of individual instructions, and wherein the script command is configured to direct the memory circuit board to:

(i) parse the payload to identify the series of individual instructions in response to the script command.

(ii) perform a series of operations in accordance with the identified series of individual instructions.

However, Lemmon has taught (and supported a well known concept), that some amount of overhead is required for every data transfer that is required. A person of ordinary skill in the art would have recognized that by packaging multiple items (in this case

instructions) into a single "packet" and then transmitting the packet, the overall number of data transfers will be reduced. For instance, if six instructions need to be transferred, and if one transfer may be performed every time unit, then six time units would be required to perform six individual transfers. On the other hand, if a packet is able to hold three instructions, then only two transfers will need to be made, resulting in four less time units required to perform the transfer. Clearly, the amount of transfer time is reduced, and as a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA to package multiple instructions and transfer them together.

Sharangpani has taught that an instruction packet includes a script command and a payload, the payload including a series of individual instructions. See Fig.2 and column 4, lines 54-57, and note the existence of a script command (field 220) and a payload (fields 210a-c), where the payload includes 3 instructions. Furthermore, in response to the script command, Sharangpani has taught parsing the payload to identify the series of individual instructions. See the abstract and Table 2 in column 6. Note that based on the template, the instructions and their types are determined and then they are routed to execution units. Finally, Sharangpani has taught performing a series of operations in accordance with the identified series of individual instructions. Clearly, each of the instructions in the payload will be executed by the appropriate execution units (those shown in Table 1 in column 5). A person of ordinary skill in the art would have recognized that if a packet of instructions is transmitted, then the packet must include instructions (payload), and the script (template in Sharangpani) is beneficial to have since it allows for rapid issuing of the associated instructions. Consequently, it would have

been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA in view of Lemmon to include a packet which contains multiple instructions (payload) and a template (script command).

27. Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani, as applied above, and further in view of Hennessy, as applied above.

28. Referring to claim 9, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 8. Furthermore, the method of claim 2 is performed by the system of claim 9. Therefore, claim 9 is rejected for the same reasons set forth in the rejection of claim 2.

29. Referring to claim 16, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 9.

30. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani, as applied above, and further in view of Narayan, as applied above.

31. Referring to claim 10, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 8. Furthermore, the method of claim 3 is performed by the system of claim 10. Therefore, claim 10 is rejected for the same reasons set forth in the rejection of claim 3.

32. Referring to claim 17, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 15. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 10.

33. Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lemmon in view of Sharangpani, as applied above, and further in view of Abdallah, as applied above.

34. Referring to claim 13, AAPA in view of Lemmon and further in view of Sharangpani has taught a system as described in claim 12. Furthermore, the method of claim 6 is performed by the system of claim 13. Therefore, claim 13 is rejected for the same reasons set forth in claim 6. Furthermore, from the teachings of Lemmon, a person of ordinary skill in the art would have recognized that by packaging results and transferring the package at once would require less overhead than individual transfers for each result (note that Lemmon's packets include 8 bytes, i.e., multiple data items - column 2, lines 64-67). Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to package results and then transfer.

35. Referring to claim 20, AAPA in view of Lemmon and further in view of Sharangpani has taught a board as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 13.

New Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 1, 23, 25, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Lemmon and further in view of Sharangpani, as applied above.

38. Referring to claim 1, AAPA has taught in a memory circuit board that stores a cache for a data storage system, a method comprising the steps of:

a) performing a series of operations in accordance with an identified series of individual instructions. See page 2, lines 5-17 of Applicant's background.

b) AAPA has not taught receiving a communication that includes a script command and a payload, the payload including the series of individual instructions, and in response to the script command, parsing the payload to identify the series of individual instructions.

However, Lemmon has taught (and supported a well known concept), that some amount of overhead is required for every data transfer that is required. A person of ordinary skill in the art would have recognized that by packaging multiple items (in this case instructions) into a single "packet" and then transmitting the packet, the overall number of data transfers will be reduced. For instance, if six instructions need to be transferred, and if one transfer may be performed every time unit, then six time units would be required to perform six individual transfers. On the other hand, if a packet is able to hold three instructions, then only two transfers will need to be made, resulting in four less time units required to perform the transfer. Clearly, the amount of transfer time is reduced, and as a result, it would have been obvious to one of ordinary skill in the art at

the time of the invention to modify AAPA to package multiple instructions and transfer them together.

Sharangpani has taught that an instruction packet includes a script command and a payload, the payload including a series of individual instructions. See Fig.2 and column 4, lines 54-57, and note the existence of a script command (field 220) and a payload (fields 210a-c), where the payload includes 3 instructions. Furthermore, in response to the script command, Sharangpani has taught parsing the payload to identify the series of individual instructions. See the abstract and Table 2 in column 6. Note that based on the template, the instructions and their types are determined and then they are routed to execution units. Finally, Sharangpani has taught performing a series of operations in accordance with the identified series of individual instructions. Clearly, each of the instructions in the payload will be executed by the appropriate execution units (those shown in Table 1 in column 5). A person of ordinary skill in the art would have recognized that if a packet of instructions is transmitted (in order to reduce overhead, as taught by Lemmon), then the packet must include instructions (payload), and the script (template in Sharangpani) is beneficial to have since it allows for rapid issuing of the associated instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA in view of Lemmon to include a packet which contains multiple instructions (payload) and a template (script command).

39. Referring to claim 23, AAPA in view of Lemmon and further in view of Sharangpani has taught a method as described in claim 1.

a) Sharangpani has further taught that the series of individual instructions of the payload has a positional order and processing the series of individual instructions in the positional order within the memory circuit board. See Fig.2, and note that the three bundled instructions, which are ultimately processed, each have a corresponding position.
b) AAPA has taught that the processing within the memory circuit board effectuates temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system. See page 1, line 7, to page 2, line 12.

40. Referring to claim 24, AAPA in view of Lemmon and further in view of Sharangpani has taught a method as described in claim 23. AAPA (in view of Sharangpani) has further taught that the step of receiving the communication includes the step of acquiring the communication including the script command and the payload, which has the series of individual instructions, from a processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload. See page 2, lines 5-9, of Applicant's background and note that each memory board may receive commands. Consequently, there must be a bus connecting each memory board to the processor board (multi-drop bus).

41. Referring to claim 25, AAPA in view of Lemmon and further in view of Sharangpani has taught a data storage system as described in claim 8. Furthermore, claim 25 is rejected for the same reasons set forth in the rejection of claim 23.

42. Referring to claim 26, AAPA in view of Lemmon and further in view of Sharangpani has taught a data storage system as described in claim 25. Furthermore, claim 26 is rejected for the same reasons set forth in the rejection of claim 24.

43. Referring to claim 27, AAPA in view of Lemmon and further in view of Sharangpani has taught a memory circuit board as described in claim 15. Furthermore, claim 27 is rejected for the same reasons set forth in the rejection of claim 23.

44. Referring to claim 28, AAPA in view of Lemmon and further in view of Sharangpani has taught a memory circuit board as described in claim 27. Furthermore, claim 28 is rejected for the same reasons set forth in the rejection of claim 24.

45. Referring to claim 29, AAPA in view of Lemmon and further in view of Sharangpani has taught a processor circuit board as described in claim 22. Furthermore, claim 29 is rejected for the same reasons set forth in the rejection of claim 23. Also, looking at Fig.4B of Sharangpani, it can be seen that the instructions within each packet (bundle) are outputted and executed (executed from left to right).

46. Referring to claim 30, AAPA in view of Lemmon and further in view of Sharangpani has taught a processor circuit board as described in claim 29. Furthermore, claim 30 is rejected for the same reasons set forth in the rejection of claim 24.

Response to Arguments

47. Applicant's arguments filed on December 3, 2004, have been fully considered but they are not persuasive.

48. Applicant argues the novelty/rejection of claim 1 on page 19 of the remarks, in substance that:

> "In Sharangpani, there is no disclosure of a method, which is performed in a memory circuit board that stores a cache for a data storage system, having a step of performing a series of operations in accordance with an identified series of individual instructions parsed from a payload of a communication having both a script command and the payload, as recited in claim 1. Rather, Sharangpani discloses a microprocessor architecture for routing instructions from an instruction buffer 320 to execution units in a subsequent stage of a pipeline 300 (e.g., see column 6, lines 42-49 and Fig. 3 of Sharangpani)."
>
> "Sharangpani does not disclose performing a series of operations in accordance with a series of individual instructions 210a, 210b, 210c. To the contrary, Sharangpani discloses routing the instructions 210a, 210b, 210c from an instruction buffer 320 to different execution units (e.g., see column 4, lines 64-67, of Sharangpani)."

49. These arguments are not found persuasive for the following reasons:

a) Firstly, regarding the first argument, due to the broad language of the claims, Sharangpani has taught a memory circuit board in that a cache is disclosed, which is a form of memory (column 7, lines 12-14) and clearly this cache will be on a circuit board. Therefore, the at least a portion of the chip of Sharangpani is interpreted as a memory board (i.e., a board with memory).

b) Regarding the second argument, applicant is correct that Sharangpani has taught the routing of instructions. However, the instructions are inherently executed (the system performs operations based on these instructions).

50. Applicant argues the novelty/rejection of claim 8 on pages 21-22 of the remarks, in substance that:

> "...the Office Action then contends that Sharangpani teaches that an instruction packet includes a script command and a payload, the payload including a series of individual instructions (see the first sentence at the top of page 10 of the Office Action). This contention is wrong. Sharangpani does not teach the use of packets. Furthermore, Sharangpani does not teach the use of instructions within a memory circuit board of a data storage system. As explained above in connection with claim 1, Sharangpani teaches routing instructions to different execution units within a microprocessor architecture."

51. These arguments are not found persuasive for the following reasons:

a) The examiner asserts that Sharangpani does in fact teach the use of packets. See Fig.2. Clearly, this is a packet (bundle) of instructions. Applicant does not specifically define, in the claims, what is meant by a packet, and therefore, the examiner is to take the broadest possible interpretation of "packet". Furthermore, as described above, Sharangpani does teach the use of instructions within a memory circuit board of a data storage system. Again, applicant gives no definition within the claims for "memory circuit board". The examiner asserts that the broadest and current interpretation taken of "memory circuit board" is a circuit with memory. Sharangpani has taught that his system may contain a cache, which is a form of memory. See column 7, lines 12-14. This memory is inherently on a chip (board). Therefore, Sharangpani has taught a memory circuit board.

52. Applicant also argues the rejections of claims 15 and 22 using the same reasons set forth in the arguments for claim 8. Consequently, the examiner responds to these arguments in the same manner as above for claim 8.

Conclusion

53. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
January 18, 2005

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